This column provides examples of cases in which students have gained knowledge, insight, and experience in the practice of chemical engineering while in an industrial setting. Summer interns and coop assignments typify such experiences; however, reports of more unusual cases are also welcome. Description of analytical tools used and the skills developed during the project should be emphasized. These examples should stimulate innovative approaches to bring real world tools and experiences back to campus for integration into the curriculum. Please submit manuscripts to Professor W. J. Koros, Chemical Engineering Department, University of Texas, Austin, Texas 78712.

SEMICONDUCTOR WAFER FABRICATION

An Opportunity for Chemical Engineers

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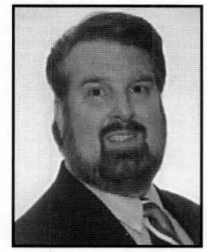
The electronics industry is a vibrant industry and one that is vital to the U.S. economy. In fact, it is the largest basic industry in the U.S., ahead of chemicals, vehicles, and petroleum refining. Electronics is also the fastest growing manufacturing industry (projected to make up 25% of total U.S. manufacturing in 1995) and the largest industrial employer in the U.S. (see Figure 1). When thinking of what technical expertise the electronics industry typically employs, electrical and computer engineers typically come to mind, but a major portion of the industry, circuit manufacturing (aka, wafer fabrication), relies heavily on physics, chemistry, and chemical engineering majors to serve as process engineers.

Wafer fabrication, the manufacturing of the microelectronics circuits that permeate every aspect of our lives today, is one of the most (if not *the* most) leading-edge manufacturing technologies in existence. Strong competition from within and abroad ensures that this technology remains on the cutting edge of development. It is so important to the U.S. economy that, since 1987, the federal government has directly funded development in this arena via contributions of $90-100 million per year to SEMATECH (SEmiconductor MAnufacturing TECHnology), a national consortium of semiconductor manufacturers. This funding is targeted specifically for enhancing the U.S. semiconductor industry's *manufacturing expertise.*

The wafer fabrication industry is currently seeing a worldwide expansion that borders on explosive growth. Industry estimates projecting the number of state-of-the-art wafer facilities to be built worldwide over the next six years approach or exceed one hundred new facilities. This phenomenal expansion is meant to address the almost insatiable hunger we have developed for microelectronics applications in all aspects of daily life.

With this level of expansion (or, taking into account the historically cyclical nature of our business, even with a much more modest estimate of fifty new facilities over the next six years) there will be a tremendous need for wafer fabrication (wafer fab) engineers. To qualify as a wafer fab engineer, one must have a good fundamental understanding of the physical nature of matter as well as strong problem-solving skills rooted in the ability to apply the scientific



***Tom Bowers** received a BS in Chemistry from the University of Texas, Austin, in 1979. He went directly into the semiconductor industry, working for Texas Instruments as a process engineer in a mature wafer fab. In 1981 he moved to Motorola to participate in a wafer fab start-up, and in 1985 he joined Advanced Micro Devices to participate in another fab start-up. He remains at AMD today, where he manages external technology transfer for its Wafer Fab Division.*

method to problem solving. Background in manufacturing techniques, process design, statistical experimental design, and control systems is viewed as an advantage. As mentioned above, individuals with either undergraduate or graduate degrees in physics, chemistry, or chemical engineering are seen as ideal candidates for wafer fab process engineers.

Unfortunately, for most physics, chemistry or chemical engineering students, this is an under-recognized career alternative. There is, however, an opportunity for undergraduate and graduate students alike to find out more about this promising career and even "try it on for size" before graduating. The industry typically offers co-op programs and some summer internships to both undergraduates and graduates. This gives students a chance to work in a wafer fab for anywhere from three months to a year or more during their education. (The co-op program at Advanced Micro Devices [AMD] is a two-semester industry commitment with traditional semesters of study at the university alternated with co-op semesters.)

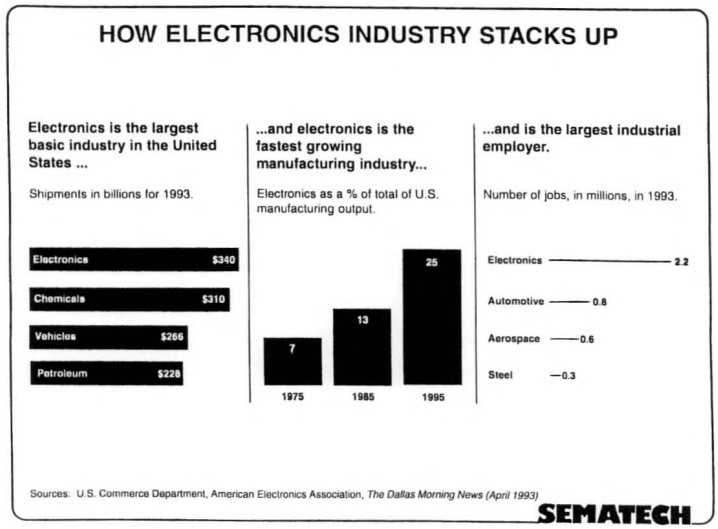


Figure 1. *Growth of the semiconductor industry.*

More details regarding AMD's co-op program will be discussed later in this article, but we will first consider examples of what, in general, is involved in wafer fabrication and how physical science and engineering skills apply to the discipline.

THE WAFER FABRICATION PROCESS

The wafer fab (*i.e.,* microelectronics fabrication facility) gets its name from the round silicon disk ("wafer") upon which the integrated circuit is built. Current leading-edge silicon wafers are 200mm in diameter by 700 microns thick and are composed of ultrahigh purity, single-crystal silicon. These wafers are the starting material for the manufacture of silicon-based integrated circuits. A typical advanced logic circuit fab will have a range of 100 to 500 devices (referred to as die) being simultaneously built on each 200mm wafer. The exact number of die depends on the total area of the individual device being built. A single advanced logic circuit at today's leading-edge technology will have four million transistors per device that must all operate within precise electrical parameters for the device to function properly.

The manufacture of these circuits on the silicon wafer entails a number of classes of operations or unit processes that, combined, produce the working device. Each of these classes of processes requires careful engineering to develop and maintain the process within required control parameters. The engineer charged with developing and maintaining any of these processes must have knowledge of specific chemical and physical aspects of the material in order to understand and control the process. The classes of operations making up the unit processes include:

Diffusion/Oxidation • These operations encompass some of the key processes in the construction of the transistor, the heart of the integrated circuit. An example of a diffusion process is the growth of the transistor's "gate" dielectric (SiO_2) in a diffusion furnace. This process is critical to transistor formation. Included in the engineering of this set of processes is knowledge of solid-state physics, quantum mechanics, solid-state diffusion laws, thermal dynamics, thermal process controls, gas-flow dynamics (at atmosphere and at millitorr pressures), crystal-lattice structures, surface interfaces and chemical bonding, surface preparation including surface roughness control and chemical contamination control (at the part-per-billion levels), surface analytical techniques, etc.

Ion Implantation • Ion implantation is the primary method of "doping" silicon (*i.e.,* introducing electrically active impurities) to change its electrical properties from those of a semiconductor to those of a conductor. Ions of materials in the III and V Periods of the Periodic Table are used as these "impurities" enabling silicon to carry electrical charges and/or pass electric current. The ion implant process involves the formation of a plasma of the "impurity" (*e.g.,* boron, phosphorus, arsenic, antimony, etc.) to be implanted. The ions in this plasma are then accelerated in a beam at high vacuum down a long mass spectrometer (which helps to purify the beam) to a wafer at the end on the beam line. When the ions hit the wafer, they are implanted into specific regions (defined by masking off regions where the ions are unwanted—see "Photolithography" below) at depths determined by the beam energy. This set of processes relies on knowledge of high vacuum, plasma chemistry and physics, physical chemistry, solid-state physics, quantum mechanics, materials science, etc.

The wafer fabrication industry is currently seeing a worldwide expansion that borders on explosive growth. Industry estimates projecting the number of state-of-the-art wafer facilities to be built worldwide over the next six years approach or exceed one hundred new facilities. . . . individuals with either undergraduate or graduate degrees in physics, chemistry, or chemical engineering are seen as ideal candidates for wafer fab process engineers.

Film Deposition • A wide range of conducting and insulating films is deposited at various points in the process. They are then patterned and etched (see "Photolithography" and "Etch" below) and new films are deposited on top of them. Typically, the films alternate between conducting and insulating layers. In this way the electrical interconnects between cells such as transistors or capacitors are made. (The complexity of the first metal layer has been described as being akin to shrinking a detailed street map of New York City down to the size of a postage stamp. Given this scale, a single defect in the film the size of a scaled-down manhole cover is enough to destroy the functionality of the die.) Common methods of deposition include physical sputtering of a material like aluminum using an inert gas such as argon, chemically reactive sputtering using a reactant gas such as nitrogen to sputter titanium and so form titanium nitride, or chemical vapor deposition of such films as polysilicon (using SiH_4) or silicon oxide (using SiH_4/O_2), etc. Engineers in this area need to develop an understanding of chemistry, physics, and material science as they apply to physical and chemical vapor deposition.

Photolithography • The patterning of those films deposited in bulk on wafers to make conducting electrical leads, for example, or the patterning of areas to be shielded from implant, is done via a process known as photolithography (typically followed by etch in the case of film patterning). The photolithography (photo) process can be broken down into two aspects. One deals with the chemistry of the photoresist polymer (resist) that is evenly coated over the surface of the wafer. This polymer is photosensitive and, when "exposed" to sufficient photon energy, breaks up into smaller chain polymers that are then soluble in a basic aqueous solution. By passing high intensity light through a chrome-on-glass mask, the light hitting the wafer can be patterned so that those areas that are "shaded" from the light remain as long chain polymers that are not soluble in the base solution. The wafer is then "developed" in the base solution, leaving resist only in the areas relating to the chrome pattern on the mask. The photoresist portion of photolithography thus clearly entails a good bit of polymer chemistry to optimize and control the process.

The other part of this process deals with the "camera," *i.e.,* the tool that houses the chrome-on-glass photomask and the light source used to "expose" the wafer. This tool, in today's technology, includes a complex set of optics that results in a five-to-one reduction of the mask pattern onto the wafer surface. This aspect of the photolithography process requires a good understanding of optics. Current challenges in this arena include optimization of optical parameters to push the use of optical lithography to its physical limits (the wave length of the monochromatic light source).

Etch • The other part of film patterning is etch. A thin film (such as a 5000 Å layer of aluminum) is first deposited across the entire surface of a wafer. The wafer then goes through the photo process described above to define precise patterns on the wafer. The wafer is then exposed to some type of etchant that attacks the film where it is left exposed (*i.e.,* not protected by the resist pattern), resulting in the film being removed from that area. Today's technology requires the use of plasma chemistry to form the reactant species used as the etchant. The wafer is placed in a plasma reactor that operates in a millitorr environment and a plasma is formed using a reactant species. For example, to etch aluminum, a chloro-carbon gas might be used to form a plasma. The chlorine ions will react with the exposed aluminum, forming aluminum chloride, a volatile compound, that is then pumped away. The result is that the aluminum film is removed from the wafer everywhere except where it was protected by the photoresist. New challenges in this field include finding new etchant species to meet environmental requirements. Clearly, plasma chemistry and plasma physics are required skills for this area.

This process summary is meant to be only a very brief overview with examples of the semiconductor manufacturing process. As such, it is greatly simplified and by no means comprehensive. The intent is to expose the reader to some of the general aspects of the process so that the reader may gain an overall appreciation for the fact that wafer fab engineering relies heavily on a basic understanding of chemistry, physics, and chemical engineering. Entry-level engineers are not expected to have these skills developed when they enter the industry, but rather to have the educational background and fundamental understanding of matter and of the scientific method of problem solving that will equip them to be able to develop these skills. A chemical engineering degree is an excellent background for entry into a wafer fab engineering position. A co-op experience in the industry further prepares graduating students and allows them to "sample" such a position virtually risk-free before making a career choice.

THE AMD CO-OP PROGRAM

With this in mind, let me now discuss Advanced Micro Devices' co-operative education program as an example

of the kind of opportunity that is available to the serious student.

AMD co-op engineering students have an exceptional opportunity to evaluate their career objectives, make professional contacts, and gain exposure to various engineering disciplines through their work experience in Sunnyvale, California, or Austin, Texas. Students involved in these programs are assigned projects by their supervisors at these facilities. The projects are not "make-work" or "junior assistant" type projects, but are truly stimulating projects that will challenge the student. The student, however, is not left alone to "sink or swim," but is mentored through the experience by his assigned supervisor. Space limitations preclude a complete recounting of the entire spectrum of co-op assignments at AMD. A short description by Jamie Mann (a senior at the University of Texas, Austin, in her third co-op rotation) of her current assignment is contained in Table 1 and should be considered as typical, but not totally representative of the breadth and depth possible in such assignments.

To participate in the co-op program at AMD, a student must

- *Maintain a grade-point average of 2.8 or above (on a 4.0 scale)*
- *Be in good standing at his or her university*
- *Be able to complete a prescribed minimum of two alternating work assignments*
- *Be a U.S. citizen or have other unlimited permission to work in the United States (permanent resident)*
- *Have completed the sophomore year (60+ hours) and have at least one term remaining upon completion of the co-op assignment*
- *Be enrolled in a BS, MS, or PhD program majoring in chemical engineering, chemistry, physics, materials science, computer science/engineering, or electrical engineering*

An interview was conducted with four current chemical engineering co-op students in AMD's Austin Wafer Fab Division to get their opinion on several aspects of the co-op experience at AMD. The students were all in their junior or senior year and ranged from first co-op semester to third co-op semester in experience. The following is a summary of their responses to selected questions.

TABLE 1
Report from a Typical Co-op Assignment

The wafer manufacturing process generates solvent wastes from several sources. These wastes flow into solvent waste lines and are collected in tanks to be disposed of properly. These solvent wastes from various sources in the wafer process mix in the solvent drain lines and may themselves react and form by-products. At AMD, these by-products clogged the drain lines and interrupted the continued operation of the wafer manufacturing facility. As a result, it became critical to identify the offending by-products, their reaction conditions, and the prevention mechanism to avoid any additional shutdown of the manufacturing process.

The inputs to the waste lines were determined from purchasing records and piping schematics. Material Safety Data Sheets (MSDS) were referenced to identify chemical constituents. The solvent wastes from the photolithography process were most suspect. In order to understand and identify probable reactions, an in-depth study of the photolithographic portion of the process was conducted. Only two reactions were identified as possible: 1) a cross-linking reaction between photoresist resins and photoactive compounds, and 2) a reaction between hexamethyl disilazane (HMDS) and photoresist solids. While a reaction between HMDS and photoresist solids is possible, the ratios in the waste stream are not favorable for this reaction and would not account for the volume of semi-solid generated.

Based on the chemistry of the species involved, it is possible and probable that a cross-linking reaction between the photoresist resins is taking place. Photoresist resins and photoactive compounds (PAC) have differing solubility characteristics. The former is relatively soluble in basic solutions while the latter is not. When the resins and photoactive compounds couple, they form a matrix that is relatively insoluble in basic solutions, nonpolar solutions, and aqueous solutions. Upon exposure to ultraviolet radiation, the photoactive compound portion of the matrix converts to an acid. The exposed matrix is then soluble in basic solutions, such as photochemical developer. The increase in solubility in basic media is the basis for photolithography. Combining the photoresist with a basic, nonpolar, or aqueous waste stream could cause the photoresist solids to precipitate out of the solution.

The possible reactions were narrowed to include the cross-linking reaction between photoresist resins and PAC and precipitation of photoresist solids due to solubility characteristics. Experimentation verified that these scenarios were the only probable ones.

At this point, AMD's internal analytical lab was consulted. Fourier transform infrared (FTIR) analysis was performed on the semi-solid and confirmed that the semi-solid was comparable to photoresist solids. However, the photoactive compound was not present in each sample analyzed. The semi-solid was also analyzed by one of AMD's suppliers. Their results described the semi-solid as comparable to the decomposition products of photoresist.

Based on the chemistry of the species involved, literature information, and analytical results, the semi-solid was identified as photoresist solids. It was determined that the photoresist solids were precipitating due to insolubility in the bulk-waste stream. The insolubility was determined to be due to the base and high alcohol content of the bulk-waste stream.

To prevent the semi-solid from forming, two possible solutions were identified: segregate the photoresist waste stream from the basic waste stream, or segregate the alcohol waste stream. The current piping system could be "broken" at the juncture and routed to two separate tanks—one for the basic input and one for the photoresist input. A more desirable solution would be to segregate the alcohol input and reprocess (recycle) it, resulting in material cost savings, disposal cost savings, and waste minimization. Implementation of either solution prevents further interruption of the manufacturing line.

While the threat to the manufacturing line was the immediate and overriding concern, understanding the nature of the problem was critical. As a result of this project, increased awareness of the process chemistry provides a basis for understanding the behavior of the waste streams and for identifying potentially incompatible materials BEFORE introduction into the waste stream.

Q What attracted you to a co-op program?

A *I thought that it would be a good experience to find out what the real world was like. I want to go into industry and need experience to determine what area I want to choose, and to be sure that I really want to be a chemical engineer. Also, the experience looks good on a resume, and it sure helps finance my education.*

Q What attracted you to the semiconductor industry?

A *I didn't know what a chemical engineer does outside the oil and gas industry and I wanted to explore other options. The semiconductor industry is not the first place you think of for chemical engineers, and I was curious to see what it has to offer. It is an expanding industry with opportunity for career development.*

Q What are you doing in your assignment at AMD?

A *1) I'm investigating a new liquid particle counting sensor technology, analyzing and interpreting data, and determining the feasibility of this technology.*

2) I'm installing defect detectors in various types of vacuum equipment for real-time process monitoring. This gives me the opportunity to learn a number of processes.

3) I'm involved in the manufacturing quality improvement of a photoresist developer solution. This includes troubleshooting process problems, working with wafer fab designers on bulk chemical distribution and its effect of fab design, and determining requirements for a new chemical services lab.

4) I'm working with product engineering in electrical yield analysis of the finished devices, including work in design layout of electrical test structures and process and device modeling.

Q How does the co-op program affect your studies when you return to classes?

A *Co-oping gives you extra incentive or motivation to learn. You now understand what you need to know and can answer the question, "Why in the world am I doing this?" The classes, in turn, help clear up some of the "fuzzy" aspects of the work experience; you can see how the course materials relate to what you have done at work and apply the subject to the "big picture." Seeing these applications makes what you are studying more interesting. The co-op experience also gives you a nice break from the pressures of school and provides financial help, which allows you to concentrate more on your studies (and less on earning money).*

Q What have you liked best about the co-op experience?

A *I have learned so much about the semiconductor industry that I never would have learned. Also, having been exposed to the professional working environment, I now know what to expect. I was surprised at the variety of projects I've been given, including working on teams made up of people of different backgrounds, age levels, and educational levels involved in real-world applications. I probably like the people I work with best—the variety of people and backgrounds.*

Q What have you liked least about the co-op experience?

A *I'm frustrated trying to overcome the concept on campus that this industry is only for EE's.*

Q What has been the biggest surprise about the experience?

A *The industry has such a laid-back atmosphere—casual dress, first-name basis (even managers), open-door office policy. I expected it to be a lot harder, all work and no fun. I found the atmosphere more laid back and not as stressful as school. I've learned that I can do this and really enjoy it. It's not as impossible as it sometimes seems in class.*

Q Would you recommend a co-op program in the semiconductor industry for others?

A *Yes, definitely. Everyone should co-op if they have the opportunity, especially if they want to go into industry. The co-op experience sets you apart from the mainstream when interviewing. The semiconductor industry is a growth industry with a lot of potential for a permanent career, especially in light of the possible engineering shortage. I would also recommend AMD very highly. AMD is a good company to work for; I really enjoy the people. AMD's business is expanding; it will have a lot of opportunities as it grows.*

Finally, some mention should be made of how a hiring manager views a co-op experience on a candidate's resume, especially when comparing that candidate to one with no co-op experience. The co-op student is generally viewed as the more serious, more mature student. He/she is not seen as a "fresh-out," but rather as someone with work experience in the industry. In fact, when the student returns to academic study after a tour in industry, that student's gain is actually recognized as more than just the time spent working in the industry. Experience shows that the student who has been in the co-op program is a better student who understands how his or her studies will be applied in the real world and, therefore, is more eager to make use of the opportunity to learn those skills essential to a successful career.

REFERENCES

1. "SEMATECH, How Electronics Industry Stacks Up," presentation given 1/19/95. ❐