LAB-BASED UNIT OPERATIONS IN MICROELECTRONICS PROCESSING

CHIH-HUNG (ALEX) CHANG, MILO D. KORETSKY, SHO KIMURA, SKIP ROCHEFORT, CYNDIE SHANER
Oregon State University • Corvallis, OR 97331-2702

The semiconductor industry has grown rapidly in the last three decades, and chemical technologies have played a central role in its continuing evolution. Historically, chemical engineering has focused on petrochemical and bulk chemical production, but more and more chemical engineers are working in the microelectronics and related industries. The most recent AIChE placement survey shows that the number of BS graduates placed in the electronics industry has increased since 1998 from 7.0% to 15.9% in 2001 (it decreased dramatically last year to 4.2% due to the economic slowdown).

The percentage of ChE graduates with advanced degrees hired into the semiconductor industry is even larger. For example, more than 25% of PhD graduates have been hired by the electronics industry since 2000.[1] Chemical engineers have the advantage of a solid background in chemical kinetics, reactor design, transport phenomena, thermodynamics, and process control that allows them to meet the challenges in microelectronics processing.

The most recent AIChE placement survey shows that the number of BS graduates placed in the electronics industry has increased since 1998 from 7.0% to 15.9% in 2001

Many chemical engineering pioneers in this field have recognized this symbiotic relationship[2-4] and a number of schools have started incorporating microelectronics processing into their curriculum. For the most part, however, the material tends to be presented in specialized, elective courses without a laboratory component. One common approach to provide hands-on experience is to have students make a transistor in a lab typically offered by the electrical engineering department. Students go through a series of microfabrication processes (either hands-on or observed) to build a complete integrated circuit, or a set of test transistors.

While this lab can be an exciting and successful approach to introduce the students to the field of microelectronic processing, there are some limitations. First of all, it is often taught with a cookbook approach, and second, there is limited time devoted to each process, so process analysis is usually ignored. The resulting device functionality supersedes the process engineering. Finally, not all schools have the necessary resources to offer this lab to their chemical engineering undergraduates.

A complementary approach is to incorporate the unit operations in microelectronics processing into the existing chemical engineering curriculum. An example of such an approach is the incorporation of thermal oxidation of silicon into the unit operations lab at Georgia Tech.[5] This approach can provide students with depth as well as breadth by presenting these unit operations in the context of core chemical engineering science.[6,7]

***Chih-hung (Alex) Chang** is Assistant Professor of Chemical Engineering at OSU. He received his BS degree from National Taiwan University and his PhD degree from the University of Florida, both in chemical engineering. His research interests include phase equilibria, photovoltaics, X-ray absorption, fine structure, electronic materials, and nano- and microtechnology.*
***Milo D. Koretsky** is Associate Professor of Chemical Engineering at OSU. He received his BS and MS degrees from UCSD and his PhD from UC Berkeley, all in chemical engineering. His research interests are in thin film materials processing, including plasma etching, chemical vapor deposition, electrochemical processes, and chemical process statistics.*
***Sho Kimura** is Professor of Chemical Engineering at OSU. His research interests cover high-temperature materials synthesis, nano-sized materials synthesis, surface modifications, applications of high-temperature fluidization technology, reaction kinetics, catalytic effects on gas-solid reactions, and reactor design and simulations.*
***Skip Rochefort** is Associate Professor of Chemical Engineering at OSU. He received his BS degree from UMass, his MS degree from Northwestern, and his PhD from UCSD, all in chemical engineering. His research interests are in all areas of polymer engineering and science and in engineering education.*
***Cyndie Shaner** served as the Linus Pauling Distinguished Engineer at OSU from 2000 to 2002. She received her BS degree in chemical engineering from Northwestern University and has had 22 years industrial experience with Chevron.*

© Copyright ChE Division of ASEE 2003

Development of programs in this area has led to innovative and improved education practices.[8-10] A successful example is the curriculum developed by the Chemical and Materials Engineering Department at San Jose State University. The essence of their project is to abandon the traditional laboratory cookbook instruction method and create a team-oriented and open-ended laboratory where students develop the types of skills they will later use in industry. The content of their laboratory includes having students make a field effect transistor and perform open-ended experiments to improve the process.[10]

While the approach at San Jose relies on coordination between students in three different engineering disciplines (electrical, material, and chemical), at Oregon State University (OSU) we are implementing the same type of learning environment solely within chemical engineering. In this way, we can leverage off the fundamental research in microelectronics processing to develop unit operations accessible to undergraduate students based on their core engineering science background.

Integration of unit operations into microelectronics has occurred in conjunction with a transformation in the senior unit operations laboratory that began during the 2000-2001 academic year. A newly created endowed chair, the Linus Pauling Engineer, was hired from industry to identify and incorporate the highest priority professional practices in the senior lab. She serves as "project director" for this class that helps graduates become prepared for industrial practice. Professional practices are incorporated into the lab through lectures, classwork assignments, and homework assignments. Eight lectures cover project management, meeting skills, technical writing, oral presentations, safety, rational management processes (situational, problem, decision, and potential problem analysis), personality self-assessment, and conflict resolution.[11] All students complete writing assignments and oral presentations to practice the professional skill as well as to demonstrate technical understanding of the unit operation. The instructor, the student, and the student's peers assess each student's work process skills, safety performance, and team behavior.

TABLE 1
Unit Operations in Microelectronic Device Fabrication

Unit Operations	*ChE Core Courses*
Bulk Crystal Growth from Melt	Fluid Dynamics; Heat Transfer; Mass Transfer; Thermodynamics; Reaction Engineering; Process Control
Surface Reactions Cleaning and Oxidation	Kinetics; Fluid Dynamics; MassTransfer
Etching Plasma Etching, Wet Etching	Mass Transfer; Kinetics; Reaction Engineering; Process Control
Thin Film Deposition • Physical Vapor Deposition • Chemical Vapor Deposition • Electrochemical Deposition	Kinetics; Fluid Dynamics; Mass Transfer; Heat Transfer; Thermodynamics; Electrochemical Engineering; Reaction Engineering; Process Control
Lithography • Photoresist spin coating • Photoresist baking • Photoresist exposure and development	Fluid Dynamics; Mass Transfer; Polymer Rheology; Kinetics; Process Control
Doping and Dopant Redistribution • Ion Implantation • Thermal Diffusion	Mass Transfer; Heat Transfer; Process Control
Planarization • Chemical Mechanical Polishing	Fluid Dynamics; Mass Transfer; Electrochemical Engineering; Process Control

INTEGRATION OF MICROELECTRONICS UNIT OPERATIONS INTO THE CHE CURRICULUM

Hundreds of individual process steps are used in the manufacture of even simple microelectronics devices, but the fabrication sequence uses many of the same unit processes a number of times. A list of unit operations that are common for the fabrication of microelectronic devices, along with the curricular material related to each topic, are given in Table 1. These unit operations rely on core chemical engineering science.

We are developing unit operations modules for integration into the chemical engineering curriculum and unit operations laboratories at OSU, including plasma etching, chemical vapor deposition (CVD), spin coating, electrochemical deposition, and chemical mechanical planarization (CMP). These unit operations contain complex systems that involve interaction of many physical and chemical processes. Fortunately, there have been extensive research efforts in these areas, and many of the fundamental mechanisms have been elucidated. For example, plasma etching processes have been modeled based on the fundamental transport and reaction processes occurring within the glow discharge to understand issues of etch rate, selectivity, uniformity, and profile.[12-15] Similarly, chemical vapor deposition reactors have been modeled in analogy to porous catalysts,[16] incorporating transport and reaction processes.[17-20] Control schemes have been based on the fundamental CVD reactor models.[21] The fluid dynamics of photoresist spin coating has been modeled and studied experimentally to predict coating thickness and uniformity as a function

of spin-speed, fluid properties, and spin duration.[22-25] Similarly, fluid-dynamics-based models of chemical mechanical polishing are being developed.[26-28]

We are synthesizing the research results in the literature and applying them to the five unit operations discussed above to make them accessible to undergraduate chemical engineers. At the same time, we are reinforcing the fundamental engineering science taught in the curriculum. To accomplish this objective, we are developing both *lab based* and *classroom based* instruction.

Integration into the lab occurs through the two required unit operations laboratories (ChE 414 and 415) as well as an elective, Thin Film Materials Processing. The first quarter of the two-quarter lab sequence is highly structured and focuses on the students completing three unit operation experiments. We intend to have each student complete at least one microelectronics unit operation during this rotation. The second quarter of the senior lab course builds on the work done in the first quarter. The focus is on working independently, developing a project proposal, completing experimental work, and writing a final technical memorandum that includes recommendations for future work. The microelectronics unit operations are designed to be flexible enough so that each year the group of students has a new, unique, and creative experience. The first four unit operations were integrated into the second-quarter lab in the spring of 2002 and are described below. The unit operations experiment in chemical mechanical planarization was added in the spring of 2003.

Students who are interested in pursuing high-tech careers can obtain a transcript visible microelectronics or materials science and engineering option in the chemical engineering department. In either of these options, Thin Film Materials Processing is required. Starting in the winter of 2003, the thin films course was expanded from 3 to 4 credits to enhance the laboratory component and in the lab the students rotated through six experiments. Three experiments—plasma etching and spin coating, silicon nitride deposition, and copper electrodeposition—are based on the unit operations mentioned earlier. Students also study wet and dry silicon oxidation, have a vacuum components lab, and undergo a "virtual" lab based on the semiconductor device applets developed by Wie and coworkers at SUNY, Buffalo.[29]

In the processing labs (plasma, CVD, electrodeposition, and oxidation), students are introduced to the unit operations. For efficacy, these labs are conducted in a well-prescribed manner where the process parameters and lab procedure are given to the students. Each group runs the process at different parameter settings, and once the entire class has rotated through a given unit operation, the students are presented with the data collected from the entire class for analysis.

For example, the silicon nitride deposition is operated at three temperatures and three flow rates (NH_3 rich, stoichiometric, and NH_3 lean). Students measure growth rate, film thickness (from which they calculate den-

Reactor Design
ChE 432 Detailed Design Project - LPCVD Silicon Nitride

Spring, 2002

Introduction
This project is designed for senior students in ChE 432 who are interested in experiencing a detailed design/simulation project in microelectronics processing. The topic selected is LPCVD (Low Pressure Chemical Vapor Deposition) that has been used for the deposition of silicon nitride on silicon wafers in the process for producing ICs.

Requirements
Students who work on this project are required to

1. Propose a design idea for a piece of equipment that handles 200 silicon wafers of 300mm in diameter
2. Develop a model to simulate the performance of the equipment
3. Determine proper operating conditions, *i.e.*, temperature distributions, operating pressure, feed rates, and reaction time for controlling the deposit thickness at 1000Å with variations across wafers and from wafer to wafer within ±3%.

Figure 1. *The CVD senior design-project assignment.*

TABLE 2
Implementation Grid of Microelectronics Unit Operations and ChE Classes

Course	*Plasma Etching*	*Chemical Vapor Deposition*	*Spin Coating*	*Electro-chemical Deposition*	*Chemical Mechanical Polishing*
Materials Balances		X			X
Energy Balances					
Chemical Process Statistics	X				
Thermodynamic Properties & Relationships	X			X	
Phase and Chemical Reaction Equilibrium		X		X	X
Applied Momentum and Energy Transfer			X		
Chemical Engineering Laboratory I		X	X	X	
Chemical Engineering Laboratory II	X	X		X	X
Chemical Plant Design I					X
Chemical Plant Design II		X			
Chemical Reaction Engineering	X	X		X	
Thin Film Materials Processing	X	X	X	X	X
Polymer Engineering and Science			X		

sity), and index of refraction for their particular run. Then they look at the entire data set of the (nine) groups in the class to explore the effect of temperature and concentration on nitride deposition.

The vacuum lab gives students experience with constructing a vacuum system and shows them the basic components in any vacuum system, including pumps, pressure measurement, mass flow control, and different types of flanges. The virtual lab provides a workshop on carrier physics, crystal structure, and integrated circuit processing with subtractive pattern transfer. For more detail, go to <jas2.eng.buffalo.edu/applets/>.

Classroom examples are developed based on the labs as well as the research literature. Each of the four unit operations listed above will include at least two example exercises or homework problems to be integrated into a core chemical engineering science or design course. By integrating the technical content in this manner, the future process engineers in this industry will be able to draw upon core fundamentals as they go about problem solving. A grid of target courses for classroom integration is given in Table 2. Those marked with an "x" represent targeted courses. For example, the design problem offered in Process Design II in the spring of 2002 is shown in Figure 1.

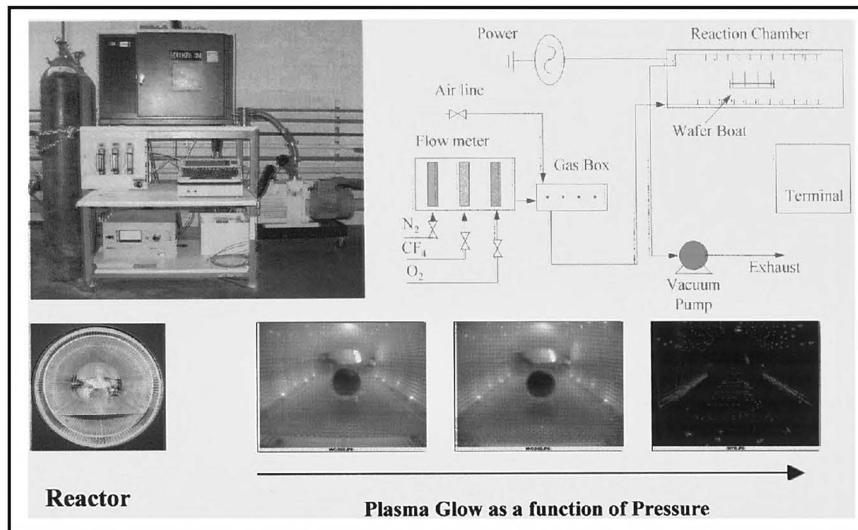


Figure 2. *Plasma barrel etcher and schematic.*

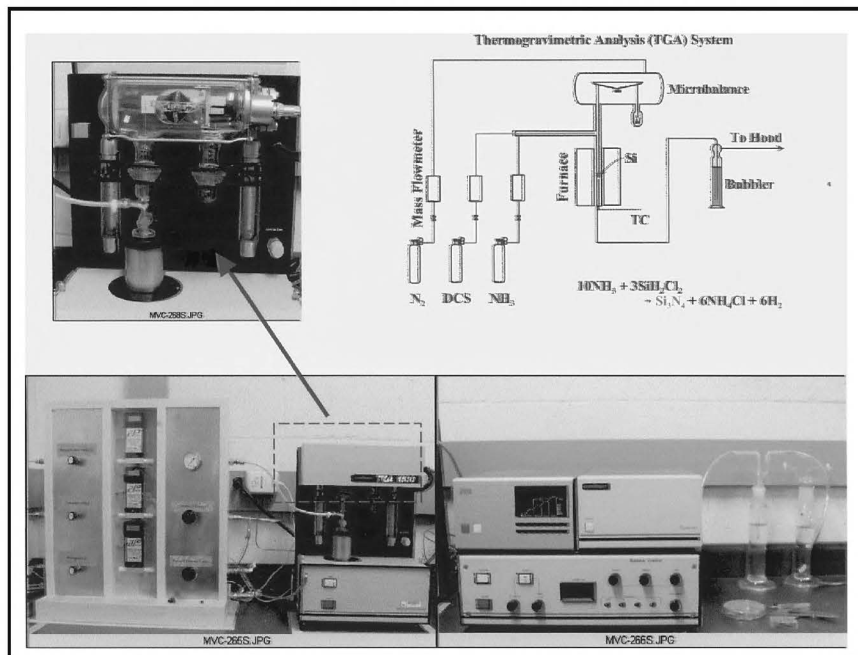


Figure 3. *Silicon nitride CVD reactor and schematic.*

■ Plasma Etching

Glow discharge plasmas are used for a variety of surface manufacturing applications, especially in integrated circuit manufacturing where up to 30% of all process steps involve plasmas in one way or another. A plasma barrel etcher has been incorporated into the projects in the second-quarter lab and the thin film course. This plasma barrel etcher unit and supporting systems were donated by Intel (see Figure 2). In the barrel etcher, ion bombardment is suppressed since the substrate holder is contained within a Faraday cage. Thus, the etch rate depends on the concentrations of free radicals that react at the substrate surface. Uniform etching only occurs when mass transport to the surface is much greater than the inherent reaction rate. By measuring the etching rate as a function of radial position, the relative importance of mass transfer to surface reaction can be backed out. The variation of etch rate as a function of the sample radius allows students to interpret etch data in terms of fundamental chemical engineering principles (*e.g.*, transport and reaction). Industrially, obtaining a uniform etching rate is also a central problem in plasma etching reactor design.

Other examples of student lab experiments include: finding optimal process settings for etching polyphenylene oxide materials using SF_6 and O_2 feed gases by using Design of Experiments (DOE) and ana-

lyzing the problem using a well-mixed reactor model; the effects of wafer spacing on etch rate; the effect of the number of substrates, *i.e.,* loading, on etch rate; and transient analysis of temperature effects on the etching rate.

In the spring of 2002, two groups of three students each were given an assignment to develop a process that minimized interwafer, as well as wafer-to-wafer, variation in etching rate. This lab included several processes to pattern and etch a wafer, including cleaning, spin coating, photolithography, and plasma etching. Additionally, students developed their own artwork to serve as a mask in photolithography. The experimental design focused on etching parameters, however, while the other processes were unchanged. One group did a 2x2 design in which they varied pressure and wafer spacing while the other group varied power and spacing. Thickness measurements before and after etching were made using a profilometer. The plasma reactor does not have temperature control. Thus the temperature rises as power is input during the etch process. This facet provided a good opportunity to use chemical engineering analysis to understand the system. The group was advised to record temperature during the process, but needed faculty help to develop an averaging method based on the Arrhenius expression for the activated process. The plasma lab analysis can be found at <http://che.oregonstate.edu/research/LBUOMEP/>.

■ Chemical Vapor Deposition

In this module, the gas-solid reaction kinetics are elucidated through real-time rate measurements using a modified thermogravimetric analyzer (TGA)(see Figure 3). Students can measure an increase in mass of the silicon wafer sample specimen (about 10 mm by 20 mm) with time, resulting from the deposition of silicon nitride at different reactant concentrations and reaction temperatures at atmospheric pressure. Inert argon is mixed with the two gaseous reactants (ammonia and dichlorosilane). Since the reaction is at atmospheric pressure, as opposed to vacuum, students must account for the effect of resistance to diffusion through the gas film on the silicon surface and find ways to eliminate the mass-transfer effects. In this context, they were asked to discuss the difference between the low-pressure CVD and atmospheric-pressure CVD. The kinetics obtained using the modified TGA were integrated into the senior capstone design course via designing a CVD reactor and simulating its performance for achieving uniform film thickness. Students were challenged to develop a simple mathematical model that incorporates the fluid flow, diffusion, and reaction that take place simultaneously. Students used their model to predict the growth of silicon nitride films on two hundred 300-mm wa-

(a)

(b)

Spin Coating of Photoresist—Fluid, Mass, and Heat Transfer Problems
Spin coating of photoresists is found in most photolithography steps in microelectronics processing. One general formulation of photoresist involves a low molecular weight polymer dissolved in a low boiling point (high vapor pressure) solvent at various concentrations (typically 60-80wt% polymer). The photoresist is spun onto a *silicon wafer* (currently 6-, 8-, or 12-inch nominal diameter) at various *spin speeds* for various *spin times*. The material properties (such as the viscosity) change with time as the solvent evaporates. Typical coating thickness values after spinning are 1-5μm, with residual solvent in the film. Residual solvent removal is achieved by a high-temperature "baking" step. There are several interesting and challenging transport problems that can be derived from this process that are suitable for undergraduate courses. These problems are not "plug and chug" but rather require that the students reason through the physical situation and apply simplifying assumptions to arrive at reasonable *models* (see two recent textbooks by Middleman[3,34,35] for examples).

Fluid Mechanics Problem • In the industrial setting, the coating process typically begins by dispensing a "puddle" of liquid at the center of a rotating wafer. The puddle very quickly spreads to the edges of the wafer. The spreading of a "viscous drop" has been presented by Middleman.[34, p. 272] The analysis most relevant to the spin coating problem presented here was first studied by Emslie, et al.,[22] where the author assumed that the film was initially at a uniform thickness across the entire wafer and that the fluid was Newtonian and nonvolatile. These assumptions led to a rather simple model for film thickness (H) in terms of spin speed (ω), spin time (t), initial film thickness (Ho), density (ρ), and viscosity (η): $H = Ho\,(1 + 4\rho\omega^2 Ho^2 t/3\eta)^{-1/2}$. The students can be given typical values of **spin speed** (1000-5000 rpm), **spin time** (30-120 sec), **initial film thickness** (Ho ~ 100μm), **density** (800 - 1000 kg/m^3), and **viscosity** (10 - 1000 mPa-s) to generate curves of film thickness (H) vs. time (t). These calculations can be used to point out the relative importance of the various parameters in a spin coating application.

Mass and Heat Transfer Problem • The transient mass transfer problem for the rate of removal of solvent from the film during the spin coating process is a difficult problem to solve. Once again, the students are challenged to make simplifying assumptions, as was done with the fluid mechanics problem, to arrive at models that can be tested. In addition to the information given above, the students are told that there must be **90% removal of the solvent** in the spinning step. One approach to solving this problem is to start with the assumption as was made above of a uniform initial coating thickness (Ho ~ 100μm). The problem then reduces to an unsteady-state mass transfer problem, similar to solvent evaporation from a polymer film described in Middleman.[35, p. 128] The students must identify the simplifying assumptions of no internal convection, one-dimensional diffusion (thin film), and rapid exterior convection due to the high speed spinning, and *comprehend the limitations of these assumptions*. For instance, if the film is spinning at high speed and thinning, how can there be no internal convection? The residual solvent removal in the "baking" step can be modeled in a similar manner.

Figure 4. *(a) Spin coater, and (b) spin coating classroom example.*

fers, varying with temperature-profile settings, reactant feed rates, and operating pressures.

■ *Spin Coating*

Spin coating has come into widespread use in the microelectronics industry for coating the photoresists used to define patterns in the films on a silicon wafer. It will also be used in future technologies as polymers become incorporated as dielectric materials. The underlying principles of spin coating (fluid flow, fluid properties, surface phenomena) and the process itself make it a natural for inclusion in the chemical engineering curriculum. The precursors to coating, surface wetting, and adhesion are also classical problems. The spin coating of solid substrates with various viscous liquids and surface wetting phenomena (surface tension, contact angle, viscosity) is done using a "state-of-the-art" programmable laboratory spin coater from Specialty Coating Systems (SCS Model P6700) (see Figure 4a) and highly polished oxide-coated 6-inch wafers. Examples of engineering projects include: experiments on viscous, Newtonian liquids to test the Emslie model and compare data to published spin coating results for Newtonian liquids;[22] coating photoresist on silicon wafers as the first step in the photolithography process.

This unit process has been used as a project in several outreach activities. Classroom examples for momentum, heat, and mass transfer are given in Figure 4b.

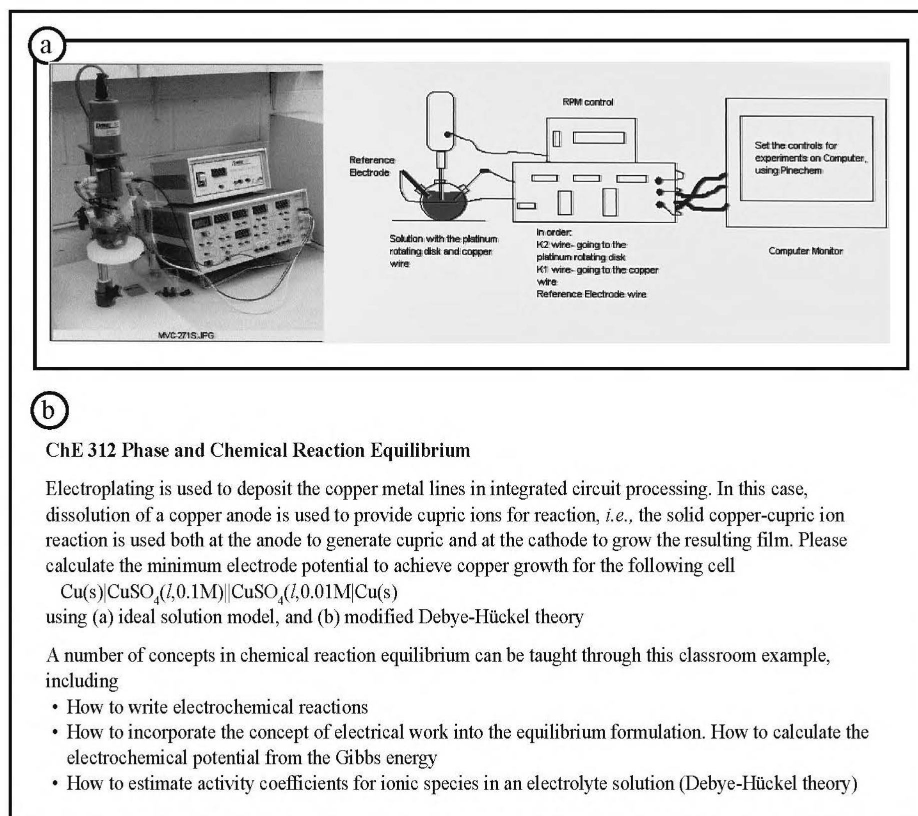
■ *Electrochemical deposition*

The electrochemical deposition system includes a computer-controlled bipotentiostat, PineChem software, rotator, electrodes, and a standard voltammetry cell (see Figure 5a). A variety of experiments could be designed using this system. Examples of such experiments are

- *Diffusion coefficient determination by rotating electrode cyclic voltammetry*
- *Measurement of the kinetics and the flux of copper ions to an electrode surface by means of rotating ring-disk electrode*
- *Study of mass transfer using rotating electrodes*
- *The effects of additives on deposition rates*
- *Leveling effects of additives*
- *Superfilling phenomena*
- *Resistive seed effect*

In the spring of 2002, the student team was taught how to use this system by going through a "cookbook" experiment using cyclic voltammetry and the rotated disk electrode to characterize the redox reaction of potassium ferricyanide solution. After the training, they were asked to propose an experimental plan using this setup. They decided to study the copper mass transport using different copper electrolytes ($CuCl_2$ and $CuSO_4$) and the influence of a sulfur-containing additive (thiourea). The experiments were performed using acid copper solutions prepared from $CuCl_2$ and $CuSO_4$ with and without thiourea. The electrochemical reactions were characterized by sweeping the voltage and measuring the current. The boundary layer thickness was controlled by the rotating speed of the working electrode and the Levich equation was used to determine the diffusivity.

A classroom example based on copper electrodeposition is given in Figure 5b. In addition, many interesting laboratory problems on copper plat-



ChE 312 Phase and Chemical Reaction Equilibrium

Electroplating is used to deposit the copper metal lines in integrated circuit processing. In this case, dissolution of a copper anode is used to provide cupric ions for reaction, *i.e.*, the solid copper-cupric ion reaction is used both at the anode to generate cupric and at the cathode to grow the resulting film. Please calculate the minimum electrode potential to achieve copper growth for the following cell

$Cu(s)|CuSO_4(l, 0.1M)||CuSO_4(l, 0.01M|Cu(s)$

using (a) ideal solution model, and (b) modified Debye-Hückel theory

A number of concepts in chemical reaction equilibrium can be taught through this classroom example, including

- How to write electrochemical reactions
- How to incorporate the concept of electrical work into the equilibrium formulation. How to calculate the electrochemical potential from the Gibbs energy
- How to estimate activity coefficients for ionic species in an electrolyte solution (Debye-Hückel theory)

Figure 5. *(a) Copper electrodeposition reactor and schematic, and (b) electrodeposition classroom example.*

ing can be found in a manuscript by Talbot.[30]

■ ***Chemical Mechanical Polishing***

The experimental setup of a bench-scale CMP module is shown in Figure 6a. The setup is adopted from the research literature,[31-33] which has been useful in understanding the reaction mechanisms during CMP. In this setup, the copper CMP will be studied in a three-electrode electrochemical cell by using a copper-plated rotating disk electrode. The polishing downward force will be measured by a balance, which supports the entire electrochemical cell. The DC electrochemical measurement will be carried out by using a potentiostat. A variety of experiments can be designed to study the copper CMP process. For example, the effect of HNO_3 or NH_4OH on the chemical etching mechanism, the effects of additives (*e.g.*, inhibitor, oxidizer), the relation between downforce, and removal rates through the Preston equation. The Preston equation[31] relates removal rate to driving force in the same way that mass transfer coefficients relate mass transfer to driving force. Studies on the bench-scale system will be scaled up to the industrial-scale system shown in Figure 6b.

OUTREACH

Three modules, including plasma etching, spin coating, and copper electrodeposition, were implemented in the outreach programs that are currently in place in the chemical engineering department: 1) Summer Experience in Science and Engineering for Youth (web site at <http://www.che.orst.edu/SESEY/>), and 2) the Saturday Academy and Apprenticeships in Science and Engineering program (web site at <http://www.ogi.edu/satacad/ASE/index.html>). Each of these programs has a somewhat different focus, but share several common underlying themes: exposure of high school students to careers in science and engineering through research experiences and other opportunities that are typically not available to them in the high schools; recruitment and retention of underrepresented groups (girls and ethnic minorities) into science and engineering; and a goal of increasing the technological literacy of high school students so they can be empowered to make educated career choices.

ASSESSMENT PLAN

The measurable student outcomes for each unit operation will include

- The students will demonstrate communication skills. *For example, they will be required to master written and oral reports.*
- The students will demonstrate technical synthesis in each of the unit operations. *For example, in CVD they will use kinetic data in reactor design problems.*
- The students will demonstrate professional practices. *For example, they will be required to demonstrate project planning before performing experiments.*

Each of these outcomes will be assessed by three methods:

- Student self-assessment and peer-assessment, *e.g.*, survey of effectiveness of educational materials.
- Evaluation of student performance by instructors.
- Feedback from industrial constituency, *e.g.*, survey of student performance from industrial employers.

SUMMARY

The integration of microelectronics-based unit operations into the chemical engineering curriculum at Oregon State University has been presented in this paper. We are developing both lab-based and classroom-based instruction. Five new unit operations are being implemented in the senior lab, including plasma etching, chemical vapor deposition, spin coat-

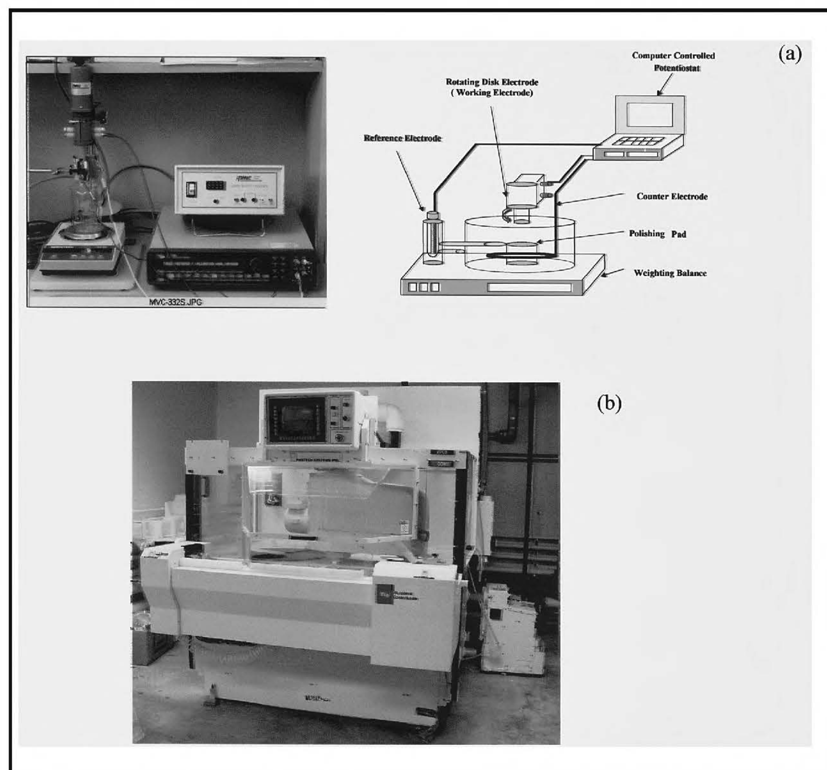


Figure 6. *(a) Bench-scale CMP and schematic (b) industrial-scale CMP.*

ing, electrochemical deposition, and chemical mechanical planarization. These labs are also included in an elective course, Thin Film Materials Processing. Classroom examples are being integrated into chemical engineering core courses. In addition, the students are learning professional practices that include effective oral and written communication, project planning, time management, interpersonal interaction, teamwork, and proactive behavior. These modules are also being used effectively in outreach programs.

ACKNOWLEDGMENTS

The authors are grateful for support provided by the Intel Faculty Fellowship Program and the National Science Foundation's Course, Curriculum, and Laboratory Improvement Program under grant DUE-0127175. We also acknowledge the Dreyfus Special Grants Program (SG-97-075), OSU Precollege Programs, Kelley Foundation, and Bridges Foundation for their support of the outreach program Summer Experience in Science and Engineering for Youth, and Pete and Rosalie Johnson for the endowment of the Linus Pauling Engineer. SEH America graciously donated the highly polished and oxide-coated 6-inch silicon wafers. Helpful discussions with Emily Allen of San Jose State University and Chuck Croy of Intel Corporation are greatly appreciated. The authors would also like to acknowledge the reviewers for the critical reading and suggestions they made regarding this paper.

REFERENCES

1. "Initial Placement of Chemical Engineering Graduates," <http://www.aiche.org/careerservices/trends/placement.htm>
2. Hess, D.W., and K.F. Jensen, eds., *Microelectronics Processing: Chemical Engineering Aspects,* Advances in Chemistry series, Vol. 221, American Chemical Society, Washington, DC (1989)
3. Middleman, S., and A. Hochberg, *Process Engineering Analysis in Semiconductor Device Fabrication,* McGraw-Hill, New York, NY (1993)
4. Lee, H.H., *Fundamentals of Microelectronics Processing,* McGraw-Hill, New York, NY (1990)
5. Hess, D.W., S. Bidstrup-Allen, P. Kohl, M. Allen, and G. May, "Thermal Oxidation of Silicon: A Unit Operation for ChEs," Session 19, ASEE Summer School for Chemical Engineering Faculty, Snowbird, UT (1997)
6. Fogler, H. Scott, *Elements of Chemical Reaction Engineering,* 3rd ed., Prentice-Hall PTR, Saddle River, NJ (1999)
7. Welty, James, Charles Wicks, Robert Wilson, and Gregory Rorrer, *Fundamentals of Momentum, Heat, and Mass Transfer,* 4th ed., John Wiley & Sons, New York, NY (2001)
8. Dang, S.S., R.A. Matthes, and C.G. Takoudis, "A Web-Based Course in the Fundamentals of Microelectronics Processing, *Chem. Eng. Ed.,* **34**(4), 350 (2000)
9. Chang, J.P., "A Hands-On Laboratory in the Fundamentals of Semiconductor Manufacturing, *Chem. Eng. Ed.,* **36**(1), 14 and references therein (2002)
10. Muscat, A.J., E.L. Allen, E.D.H. Green, and L.S. Vanasupa, "Interdisciplinary Teaching and Learning in a Semiconductor Processing Course," *J. Eng. Ed.,* **87**, 413 (1998)
11. Koretsky, M.D., C.-H. Chang, S. Kimura, S. Rochefort, and C. Shaner, "Integration of Microelectronics-Based Unit Operations into the ChE Curriculum," Session 1313, Proceedings of the 2003 ASEE Annual Conference
12. Bell, A.T., "Fundamentals of Plasma Chemistry," in *Techniques and Applications of Plasma Chemistry,* A.T. Bell and J.R. Hollahan, eds., John Wiley & Sons, New York, NY (1974)
13. Graves, D., and K.F. Jensen, "A Continuum Model of DC and rf Discharges," *IEEE Trans. Plasma Sci.,* **P5-14,** 78 (1986)
14. Alkire, R.C., and D.J. Economou, "Transient Behavior During Film Removal in Diffusion-Controlled Plasma Etching," *J. Electrochem. Soc.,* **132,** 648 (1985)
15. Plumb, I.C., and K.R. Ryan, "A Model of the Chemical Processes Occuring in CF_4/O_2 Discharges Used in Plasma Etching," *Plasma Chem. Plasma Proc.,* **6**, 231 (1986)
16. Levenspiel, O., *The Chemical Reactor Omnibook,* Oregon State University, Corvallis, OR (1993)
17. Hess, D.W., K.F. Jensen, and T.J. Anderson, "Chemical Vapor Deposition: A Chemical Engineering Perspective," *Rev. Chem. Engg.,* **3**, 97 (1985)
18. Jensen, K.R., and D.B. Graves, "Modeling and Analysis of Low Pressure CVD Reactors, *J. Electrochem. Soc.,* **130**, 1950 (1983)
19. Roenigk, K.F., and K.F. Jensen, "Low Pressure CVD of Silicon Nitride, *J. Electrochem. Soc.,* **134**(7), 1777 (1987)
20. Fogler, H. Scott, *Elements of Chemical Reaction Engineering,* 3rd ed., Prentice-Hall PTR, 789 (1999)
21. Edgar, T.F., S. Butler, W.J. Campbell, C. Pfeiffer, C. Bode, S.G. Hwang, K.S. Balakrishnan, and J. Hahn, "Automatic Control in Microelectronics Manufacturing: Practices, Challenges, and Possibilities," *Automatica,* **36**, 1567 (2000)
22. Emslie, A.G., F.T. Bonner, and L.G. Peck, "Flow of a Viscous Fluid on a Rotating Disc," *J. Appl. Phys.,* **29**, 858 (1958)
23. Flack, W.W., D.S. Soong, A.T. Bell, and D.W. Hess, "A Mathematical Model for Spin Coating of Polymer Photoresists," *J. Apply. Phys.,* **56** 1199 (1984)
24. Bornside, D.L., C.W. Macosko, and L.E. Scriven, "Spin Coating: One-Dimensional Model," *J. Apply. Phys.,* **66**, 5185 (1989)
25. Strong, L., and S. Middleman, "Lubricant Retention on a Spinning Disk," *AIChE J.,* **35**(10), 1753 (1989)
26. Subramanian, R.S., and L. Zhang, "Some Transport Phenomena Issues in Chemical Mechanical Polishing," 3rd Annual Workshop on Chemical Mechanical Polishing (1998)
27. Runnels, S.R., and L.M. Eyman, "Tribology Analysis of Chemical Mechanical Polishing," *J. Electrochem. Soc.,* **141**, 1698 (1994)
28. Stein, D.J., D.L. Hetherington, and J.L. Cecchi., "Investigation of the Kinetics of Tungsten Chemical Mechanical Polishing in Iodate-Based Slurries," *J. Electrochem. Soc.,* **146**, 376 (1999)
29. <http://jas2.eng.buffalo.edu/applets/>
30. Talbot, J.F., "Electrochemical Engineering in the Process Laboratory Course," *Chem. Eng. Ed.,* **35**(1), 74 (2001)
31. Steigerwald, J.M., S.P. Murarke, and R.J. Gutman, *Chemical Mechanical Planarization of Microelectronic Materials,* John Wiley & Sons, New York, NY (1997)
32. Tsai, Tzu-Hsuan, and Shi-Chern Yen, "Electrochemical Effects of Various Slurries on the Chemical Mechanical Polishing of Copper-Plated Films," submitted to *J. Electrochem. Soc.*
33. Kneer, E.A., C. Raghunath, V. Mathew, and S. Raghavan, "Electrochemical Measurements During the Chemical-Mechanical Polishing of Tungsten Thin Films," *J. Electrochem. Soc.,* **144**, 3041 (1997)
34. Middleman, S., *An Introduction to Fluid Mechanics: Principles of Analysis and Design,* John Wiley and Sons, New York, NY (1998)
35. Middleman, S., *An Introduction to Mass and Heat Transfer: Principles of Analysis and Design,* John Wiley & Sons, New York, NY (1998) ❐