WORKING IN THE INTEGRATED CIRCUIT INDUSTRY

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CAROL M. McCONICA received her PhD (1982) in chemical engineering from Stanford University. She spent three years with Hewlett Packard (1979-1982) developing state-of-the-art deposition/etching processes for their 128Kb RAM and 640Kb ROM, all fabricated with 1 micron NMOS double-layer metal technology. She is currently an associate professor at CSU leading a graduate program in IC processing.

THE INTENT OF THIS article is to introduce you to the work environment and the culture in the IC (integrated circuit) industry. This introduction to the work environment is necessary to adequately prepare you for making a career choice. In each of the paragraphs below, a statement of fact about the industry will be given and then discussed in terms of how it creates a culture or a unique work environment. A design process typical of the industry will be contrasted with chemical engineering design so that you can grasp the level of sophistication of the manufacturing environment. Lastly, the advantages of working in this industry will be highlighted.

In the IC industry, the product has an electrical engineering application, and thus the management and the majority of the employees are electrical engineers. Because electrical properties (film resistivity, electromigration properties, contact resistance, leakage current, dielectric constant, breakdown voltage, *etc.*) of materials directly relate to the material properties (grain size, contamination, stress, adhesion, alloy type, *etc.*), the second most frequently encountered employee is a material scientist. Only rarely does one find a chemical engineer in the IC industry. This distribution of employees results in a culture which considers process development and reactor design as extraneous to the primary function of the company. The most enlightened form of the industry recognizes that reactor conditions during film deposition contribute to the film properties, and the cause and effect relationships are correlated through orthogonal matrices. Because the average material scientist or electrical engineer has very little, if any, education in heat, mass, or momentum transport, in gas-solid kinetics or in reactor design, the whole problem of process design takes on the mystique of being a black art. A properly-educated chemical engineer in this environment can become an instant hero, if the stage is properly set, by applying his/her knowledge of reactor design to the manufacturing processes. But beware—any great opportunity comes with an equally great challenge.

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The product which is being manufactured is not just one chemical which has been modified through a series of processes. It is a layered structure resulting from at least 100 sequential operations, each one with the potential to influence an earlier layer or a later layer. You will be working with 50-100 other engineers, each responsible for a different set of steps in the process of building an integrated circuit. Most of these people will be trained in chip design and failure analysis, but will generally be undereducated in process design. Compound this with the fact that the product you make is not visible to the naked eye. The best analogy is of one hundred blindfolded sculptors trying to recreate Michelangelo's statue of David while it sits on a rotating table. Success is determined by an artist at the end of the process deciding if it looks like the original. Failure analysis is a process of trying to determine which piece was sculpted poorly many layers and many rotations ago.

Because the chip yield is the only true measure of the viability of a new process, all proposed processes must be demonstrated upon a real product. In a development facility there may be only ten lots (25 wafers

each) every eight weeks that are available to all 100 process engineers for development purposes. This means that any one engineer may receive only two to five patterned test wafers every two months on which to test his/her ideas. Because process interactions are so strong, the best process developed on unpatterned wafers may yield horribly on the real patterned test wafers. The best process engineers strive hard to understand the interactions within their own process, whether it be an etch step, a deposition step, or photolithography, before receiving those very few and very precious test wafers. The clever process engineer also gets his/her hands dirty and learns the details of all the steps in creating films which will be contacting his or her film. This is a job best suited to experimentalists, and if you went through school attached only to a computer, you will find your work overwhelming. You better know when vacuum pump oil can contaminate wafers and how to run a scanning electron microscope.

An interesting result of the test wafer starved environment is an underground black market for test wafers within any facility. Imagine a product market in the 1200*s* where the people bartered their goods one at a time, and after a full day on the town square they had enough to live on for the next day or two. Any IC industry is a culture of 50-100 individuals networking furiously among themselves to obtain a few test wafers so that they can get their own jobs done and become heros. Some individuals may operate through intimidation, others through bribing their friends with weekends on a family catamaran. Students simply won't need their speech classes or formal presentation skills—a much better background is in interpersonal relationships and in the art of negotiation or coercion 101.

Another interesting result from 50-100 people developing one invisible product with very strong process interactions is the "hot potato" syndrome. Imagine the case of shorts between metal lines on the chip's interconnect. Let's investigate where this failure mode might originate. It could be that conductive contamination was left during processing prior to metal deposition; or the metal itself may have an improper composition, making the etch difficult; or the photolithography process could be failing, leaving photoresist where it should not be; or the etch reactor may have changed its performance and is no longer clearing out the metal between the lines. These are the obvious possibilities. It could also be that the engineer in charge of oxide deposition (several layers ago) changed the process slightly, creating steeper sidewalls, and thus the etch can no longer clear metal from under the new geometries. Who owns the problem? Clearly, the lab manager owns the problem, just like he/she owns all of the other problems in the clean room. It is too often the case that the lab manager is faced with a group of engineers, each claiming the problem belongs to another process group—thus the "hot potato" syndrome.

IC fabrication lines are very expensive to build and operate. Therefore, companies are forced to develop new processes on equipment producing the current product. The consequences of this constraint are profound. Hardware modifications are nearly always forbidden because they may interfere with current product yield. Remember that the hardware/process interactions are so poorly understood that any hardware change is viewed as potentially dangerous. The chip manufacturers do not consider themselves in the business of inventing processes and would rather work with a low-yielding piece of hardware than to modify it to optimize its performance. Imagine a sculptor making statues out of soap when the management decides to make statues out of metal. The sculptor now has to figure out how to sculpt metal with the same old tools because the production of soap statues must not be interrupted.

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Not only is there the obvious problem of making an inadequate tool (today's batch reactor) to create a new product (tomorrow's chip set), but there is the added problem of getting time on the production machines to run tests. Today's product represents today's profit, and therefore production wafers take precedence over test wafers. Engineers have to find time for development without interfering with production. This creates another interesting situation: the art of bribing the machine operator off of the reactor for a while. (Once a chip set goes to production, it is handled almost exclusively by operators, not engineers.) Common tactics range from encouraging the operator to take long coffee breaks to designating the machine as "down," implying that it has hardware problems and is not suitable for production runs. Either method allows the engineer to process a batch of test wafers, and he/she works diligently trying to make the old tools fit the new need. Sometimes they are successful, but usually the IC industry is forced

to wait for new tools to be developed by equipment vendors.

Because the chip facilities view process development as the job of the equipment vendor, and the equipment vendor has no idea what the next generation of chips will look like, there exists a mismatch between the time a process is needed (now) and when the vendor can make a machine to fulfill this need (two years from now). The equipment companies are expected to produce the very best IC batch reactors with almost no capital investment from the IC industries. Not only is there no monetary support, but the IC fabrication engineers generally distrust equipment vendors because the last generation of batch reactors did not come with an adequate recipe for processing wafers. The vendors cannot find that optimum recipe because they do not have access to patterned wafers, which are the ultimate test of a process. In fact the IC fabs are very reluctant to help the vendor create the process because they don't want any information to leak out about the next generation of chips. As a consequence of this nearly adversarial vendor-IC fabrication facility relationship, the process becomes an orphan. The IC chip fabrication engineer is then faced with spending $1.5 million on a piece of hardware (a batch reactor useful for one step of the 100-step process) with only a vague idea of the best operating conditions for his/her chip set.

There is usually a honeymoon period, albeit a short one, where the new machine belongs to a development engineer and not yet to production. In this window of one to three months, the development engineer is given *carte blanche* on the machine and some priority on obtaining test wafers. This is where six to eight years of chemical engineering buys leverage. The advantage is best understood by contrasting the textbook chemical engineering methods of process development with the methods currently used in the industry.

For the purpose of discussion, film properties and device behavior are termed "level 1" variables in this document, for they are the important surface properties dependent upon the local chemical environment present during growth (Figure 1). These level 1 properties are most directly related to the surface composition during growth, which in most cases is unmeasurable and only roughly predictable. The only exception to this is the measurement of surface composition during growth with Raman spectroscopy or *in situ* low energy electron spectroscopy, a technique requiring vacuum capabilities in the 10^{-10} torr range. The measurable variables which most directly affect film properties are the local gas composition, the wafer

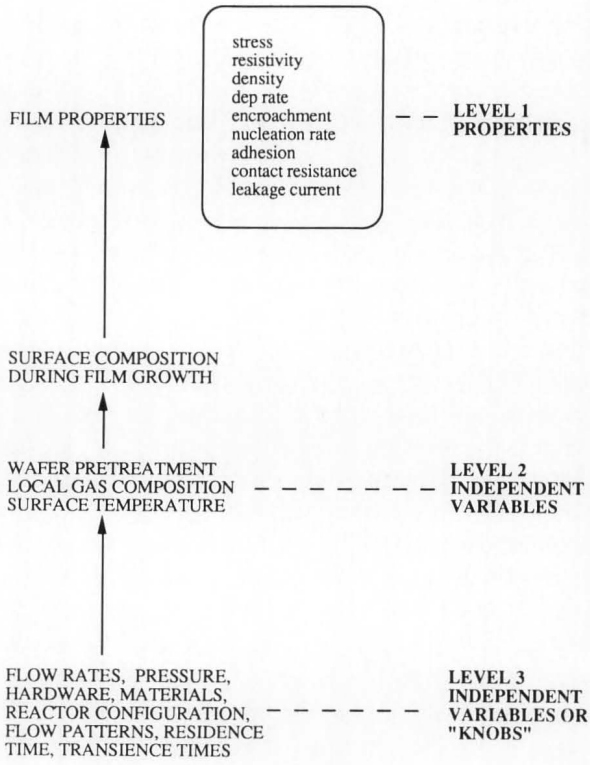

FIGURE 1. Variable chart

pretreatment, and the surface temperature—the local gas composition being that within a few mean free paths of the wafer surface. These variables are referred to as independent level 2 variables, for they control the level 1 dependent variables. Ultimately the level 2 variables are determined by the gas flow rates, pressure, reactor hardware, species residence times, reactor materials, transience times in the reactor, heating method, and other "*reactor knobs.*" It has been the tradition in the IC industry to turn the level 3 reactor knobs in an orthogonal manner in order to determine the best conditions for running a piece of hardware. The level 1 properties are related to level 3 knobs by statistical correlations without any fundamental understanding of the processes involved. It is a perfect tool for engineers with an educational mismatch to the product they are expected to build. It is, for instance, how I would go about building a strong bridge since I am not trained in stress analysis.

This method of orthogonal experimental design is very well suited to processes where nothing is known about the behavior of the process and the hardware. Plasma processes, for instance, are so complex that they have traditionally qualified for this category. For processes which are dominated by chemical reactions with known kinetics (classical chemical vapor deposition), this method is not optimal. With a few heat and

mass balances, calculations of dimensionless groups, and an understanding of kinetics a skillful chemical engineer can often solve in an afternoon what a process engineer has been statistically correlating for man-months.

For demonstration purposes, let us contrast chemical engineering reactor design to orthogonal matrix design for a semi-batch reactor with no heat and mass transfer limitations (the most primitive case). As a chemical engineer, you are aware that the film properties are dominated by the local reactant concentrations and temperature. Any reactor design text will give the appropriate design equation, depending upon the Peclet number, for the reactor. Knowing the design equation, the kinetics, and the stoichiometry, the growth rate is perfectly predictable. Level 1 properties can then be related to the actual deposition environment given by the calculated level 2 variables.

If the kinetics are unknown, a chemical engineer is aware that the variables critical to film deposition are the local concentrations and surface temperatures. At this point the engineer can choose to determine the basic kinetics and create a predictive model, or more realistically he/she will be in an industrial situation that does not allow fundamental studies and will design an experiment based upon orthogonal matrices. The key in being efficient is in realizing that the engineering staff will have a more fundamental understanding of which variables actually control material properties if the matrix is built around level 2 variables (concentrations) rather than level 3 knobs (flow rates). This approach differs dramatically from the blind approach of most process engineers in the IC industry today.

Figure 2 is a plot of the operating conditions for performing an orthogonal matrix in flow rate space, the industry standard, for reactants A, B, and C. Figure 3 shows those same operating points plotted in concentration space when given a fixed surface area for deposition. As can be seen, in concentration space (the only one that really matters) the matrix is far from orthogonal. Interpretation of the experiments in terms of fundamentals is all but impossible. In fact it is no mystery at all that the industry has so much difficulty in converging on optimal processes.

The US IC industry is battling for survival against foreign competition. If it is to survive, it will have to develop a new strategy. We are already witnessing cooperation among competing industries and vendors in the form of Sematech. To really become an international leader, the US industry will have to launch itself out of the mode of empirical correlations and base its manufacturing processes upon science. This is the very heart of chemical engineering, and chemical engineering should therefore become the very center of the future of the IC industry. It is a waste of time to have fine circuit designers attempting to derive heat transfer relationships given in junior level chemical engineering textbooks, or attempting to define kinetics based upon pseudo-orthogonal matrices. It is our responsibility to use our knowledge and our tools to solve these problems efficiently and scientifically.

For chemical engineers, the IC industry is a gold mine of opportunity. Compared with the petroleum industry, the technical problems are easy. The processes operate at low pressure and moderate temperatures. Reactors often behave as mixed flow reactors because the diffusivities are so large. Pressure drops never exist. Processes are just as likely to be kinetically limited as mass transfer is limited. The reactions are often inorganic. One is usually limited to two

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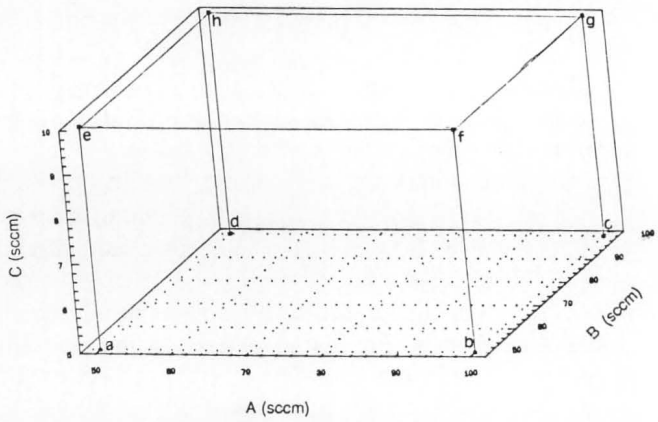

FIGURE 2. Orthogonal matrix in flowrate space for reactants A, B, and C.

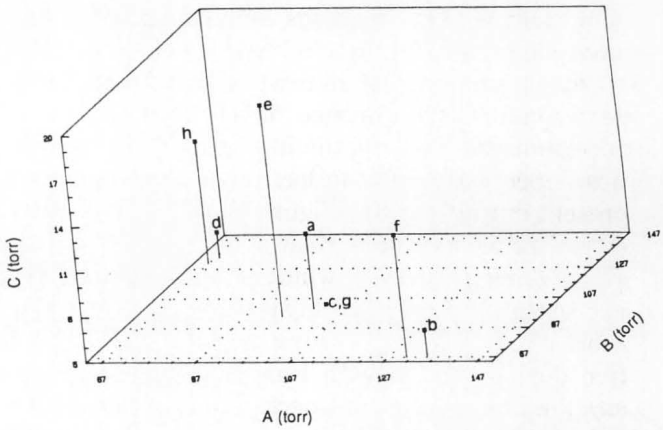

FIGURE 3. Operating points in Figure 2 plotted in partial pressure space, which is identical to concentration space when divided by the constant RT.

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with a tendency for high quality. Many of the early PhD graduates, for instance, went on to become professors and administrators at major universities.

Since the majority of graduate students in a developing program were in the MS degree program, they were very closely supervised and generally produced publication-quality work. Many have gone on to important positions: three are company vice presidents; one is a director of overseas development; and several are heads of company divisions of various types. Several others pursued PhDs at other universities and have entered academia or research and development.

As mentioned before, the PhD/MS student ratio has recently increased to a level that will ensure a high rate of PhD graduates in future years. It appears that the department is beginning to achieve its early objectives for the graduate program. In terms of doctoral students, the department has been long on quality but short on quantity. Now that graduate enrollment has reached the desired level, we are focusing our efforts on maintaining quality in both graduate and undergraduate programs. □

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phases: gas and solid. Because of problems with particulates, liquids have been all but eliminated from the clean room. The reactors are small, and a batch of product can be held in one hand. Reaction times are on the order of minutes rather than days, so the turnaround is fast. Process control is simply a matter of using *in situ* diagnostics to predict the endpoint of an etch or deposition step. Compared with the difficulties of death, mutation, complex organic chemistry, living membranes, and mass transfer limitation typical of bio-engineering, the challenges of the IC industry are controllable. The problems are straightforward, but they generally require experimental solutions. There is enough work to be done to keep surface scientists occupied for several decades. Not only do the problems require experimental solutions, but the chemical engineer who lacks knowledge of device physics is just as handicapped as the electrical engineer with his/her ignorance of continuum mechanics. The need for a cross-disciplinary education cannot be overemphasized.

In conclusion, if you have the people skills to run for congress, the patience to spend a day in a junior high school, the perseverance to climb Mt. McKinley, the hands-on skills to keep dual Weber carburetors perfectly tuned on a 1960 Porsche, and the desire to help an industry which is vital to our national security and economy, consider obtaining a graduate degree in IC processing and joining a US IC company. □